I claim:

1. A system that includes

a first pulse train input to a switch having a repeating high value and low value at a first frequency, and a transition from the low value to the high value having a first edge sharpness;

a second pulse train input to the switch in synchronization with the first pulse train having a repeating high value and low value at a second frequency lower than the first frequency;

the switch selecting an output from one of the first pulse train and the second pulse train to create an output pulse train appropriate to transition fault test an integrated circuit, depending upon a selection signal having a determined pulse train input to the switch;

the selection signal in synchronization with the first pulse train;

wherein the switch switches from the second pulse train to the first pulse train and substantially maintains the first edge sharpness of the first pulse train, and from the first pulse train to the second pulse train, during a low value of both the first and the second pulse train.

2. The system as defined in claim 1 further including

a signal input to the switch having the substantially low value;

the switch selecting an output from one of the first pulse train input, the second pulse train input, and the third input, depending upon the selection signal;

wherein the switch switches from the second pulse train to the first pulse train by switching from the second pulse train to the signal to the first pulse train.

3. The system as defined in claim 1 further including

a signal input to the switch having substantially the low value;

the switch selecting an output from one of the first pulse train input, the second pulse train input, and the third input, depending upon the selection signal;

wherein the switch switches from the first pulse train to the second pulse train by switching from the first pulse train to the signal to the second pulse train.

4. The system as defined in claim 1 wherein the selection signal consists of one of:

a third pulse train and a fourth pulse train; and

a third pulse train.

5. The system as defined in claim 1 further including

an edge placement accuracy improvement circuit to improve the edge placement accuracy of an input pulse train;

wherein the output of the edge placement accuracy improvement circuit has substantially the edge placement accuracy of the first pulse train, and the edge placement accuracy improvement circuit is coupled between the input pulse train and the switch; and

the input pulse train.

6. The system as defined in claim 5 further including a pulse train alignment circuit to align the first pulse train with the second pulse train, wherein the pulse train alignment circuit is coupled to at least one of the input pulse train-first pulse train path and the second pulse train path.

7. The system as defined in claim 1 further including

a frequency changing circuit to one of multiply and divide the frequency of an input pulse train, wherein the output of the frequency changing circuit has substantially the frequency of the first pulse train, and the frequency changing circuit is coupled between the input pulse train and the switch; and

the input pulse train.

8. The system as defined in claim 7 further including a pulse train alignment circuit coupled to at least one of the input pulse train-first pulse train path and the second pulse train path to align the first pulse train with the second pulse train.

9. The system as defined in claim 1 further including

a circuit that includes an edge placement accuracy improvement circuit and frequency changing circuit to both improve the edge placement accuracy of an input pulse train and one of multiply and divide the frequency of an input pulse train, wherein the output of the circuit has the edge placement accuracy and the frequency of the first pulse train, and the circuit is coupled between the input pulse train and the switch; and

the input pulse train.

10. The system as defined in claim 9 further including a pulse train alignment circuit coupled to at least one of the input pulse train-first pulse train path and the second pulse train path to align the first pulse train with the second pulse train.

11. The system as defined in claim 1 further including

a pulse train alignment circuit to align the selection signal with at least one of the second pulse train and the first pulse train.

12. The system as defined in claim 1 further including

a signal conditioning circuit to translate the voltage level of an output of the switch; and

the output of the switch.

13. A method that comprises:

inputting a first signal having a predetermined pulse train pattern into an input port of a switch at a frequency to load and unload a scan chain of a circuit under test;

inputting a second signal having a predetermined pulse train pattern into an input port of the switch at a functional frequency and edge sharpness to provide a transition fault testing input to the circuit under test;

inputting at least one third signal into a selection port of the switch, the third signal having pulse values determined to select a pulse from at least the first signal and the second signal to provide the switch output to the circuit under test having in sequence a first signal portion to load and unload the scan chain, and the second signal portion to exercise the circuit under test having substantially the edge sharpness of the second signal.

14. The method as defined in claim 13 wherein the selection signal is in synchronization with the second signal.

15. The method defined in claim 13 further including the third signal determining the switch output by switching from the first signal to the second signal during a low value of both the first and the second pulse train.

16. The method as defined in claim 13 further including:

inputting a fourth signal having a substantially low value into an input port of the switch;

the third signal having pulse values determined to select a pulse between at least the first signal, the second signal, and the third signal; and

wherein said selecting determines a transition from the first signal to the second signal, that includes a transition from the fist signal to the third signal to a low value of the second signal.

17. The method as defined in claim 13 further including:

inputting a fourth signal having a substantially low value into an input port of the switch;

the third signal having pulse values determined to select a pulse between at least the first signal, the second signal, and the third signal; and

wherein said selecting determines a transition from the second signal to the first signal, that includes a transition from the second signal to the third signal to a low value of the first signal.

18. The method as defined in claim 13 further including forming the second signal by inputting a signal having a less sharp edge into an edge placement accuracy improvement circuit.

19. The method as defined in claim 13 further including forming the second signal by inputting a signal having a lower frequency into a frequency multiplication circuit.

20. The method as defined in claim 13 further including aligning the first signal and the second signal.

21. The method as defined in claim 13 including aligning the second signal and the third signal.

22. The method as defined in claim 13 including adjusting the voltage value of the switch output to the voltage value of the circuit under test.

23. A system that includes:

a first pulse train at a frequency adequate to load and unload at least one scan chain of an integrated circuit input to a switch;

a second pulse train in synchronization with the first pulse train having a frequency and pulse edge sharpness adequate to test the propagation time of an integrated circuit core at functional at-frequency rates input to the switch;

the switch that dynamically outputs alternatively a portion of the first pulse train or the second pulse train as an output, based on an input from an at least one selection signal; and

the selection signal defined for the switch to output a signal to the scan chains to load and unload the scan chains and to transition fault test the integrated circuit core.

24. The system as defined in claim 23 further including:

a signal having a substantially low value input to the switch wherein the switch outputs alternatively the first pulse train portion or the second pulse train portion or the signal as an output, based on an input from the selection signal;

the switch switches the output from the second pulse train to the first pulse train by switching from the second pulse train to the signal to the first pulse train; and

the switch switches the output from the first pulse to the second pulse train by switching from the first pulse train to the signal to the second pulse train.

25. The system as defined in claim 23 further including an input pulse train and at least one of:

a smoothing circuit to improve the edge placement accuracy of the input pulse train, wherein the output of the smoothing circuit has the edge placement accuracy of the second pulse train, and the smoothing circuit is coupled between the input pulse train and the switch; and

a frequency changing circuit to one of multiply and divide the frequency of the input pulse train, wherein the output of the frequency changing circuit is the first pulse train, and the frequency changing circuit is coupled between the input pulse train and the switch.

26. The system as defined in claim 25 further including

an alignment circuit coupled to at least one of the input pulse train-second pulse train path and the first pulse train path to align the first pulse train with the second pulse train.

27. The system as defined in claim 23 further including

a calibration circuit to align the selection signal with at least one of the first and second signal.

28. The system as defined in claim 23 wherein the selection signal is in synchronization with at least one of the first signal and the second signal